ABSTRACT

A system is provided for controlling the delay in an isolation buffer. Multiple such isolation buffers are used to connect a single signal channel to multiple lines and controlled to provide an equal delay. Isolation buffer delay is controlled to be uniform by varying either power supply voltage or current. A single delay control circuit forming a delay-lock loop supplies the delay control signal to each buffer to assure the uniform delay. Since controlling delay can also vary the output voltage of each isolation buffer, in one embodiment buffers are made from two series inverters: one with a variable delay, and the second without a variable delay providing a fixed output voltage swing. To reduce circuitry needed, in one embodiment an isolation buffer with a variable power supply is provided in a channel prior to a branch, while buffers having a fixed delay are provided in each branch. A wafer test system can be configured using the isolation buffers having equal delays to enable concurrently connecting one tester channel to multiple wafer test probes.